

U.S. Patent Application Serial No. 10/577,490

MARKED-UP ABSTRACT

By: Shoji KAWAHITO et al.

Attorney Docket No.: 062487**ABSTRACT OF THE DISCLOSURE**

An A/D conversion array for an image sensor, in which the number of amplifiers and capacitors are decreased, compared with the conventional cyclic type, and a function to cancel the noise generated in the pixel section of the image sensor is provided, so that the area and power consumption are decreased. After ~~[[an]]~~ input signal V_{in} is supplied to C1 and held, a reset level is applied to V_{in} , whereby the ~~differential~~ signal is amplified by the ratio of C1 and C2 ($C1/C2$) ~~connected to an inverting amplifier~~. Then ~~[[an]]~~ An output ~~from the inverting amplifier~~ is held in C1, and the output ~~of the inverting amplifier~~ is A/D-converted by a comparator so that a control signal is generated by the conversion output, and ~~one of the~~ a switch ~~switches controlled by $\phi M1$, $\phi O1$ and $\phi P1$~~ is turned ON. The digital signal is converted into an analog signal, and the analog signal is subtracted from the signal held in C1. This signal is amplified and is subjected to A/D conversion again, ~~then and~~ and the same operation is ~~cyclically~~ repeated. By this, ~~noise cancellation and multi-bit A/D conversion can be performed.~~

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REPLACEMENT ABSTRACT

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An A/D conversion array for an image sensor, in which the number of amplifiers and capacitors are decreased, compared with the conventional cyclic type, and a function to cancel the noise generated in the pixel section of the image sensor is provided, so that the area and power consumption are decreased. After input signal V_{in} is supplied to C1 and held, a reset level is applied to V_{in} , whereby the signal is amplified by the ratio of C1 and C2 ($C1/C2$). An output is held in C1, and the output is A/D-converted by a comparator so that a control signal is generated by the conversion output, and a switch is turned ON. The digital signal is converted into an analog signal, and the analog signal is subtracted from the signal held in C1. This signal is amplified and is subjected to A/D conversion again, and the same operation is repeated.